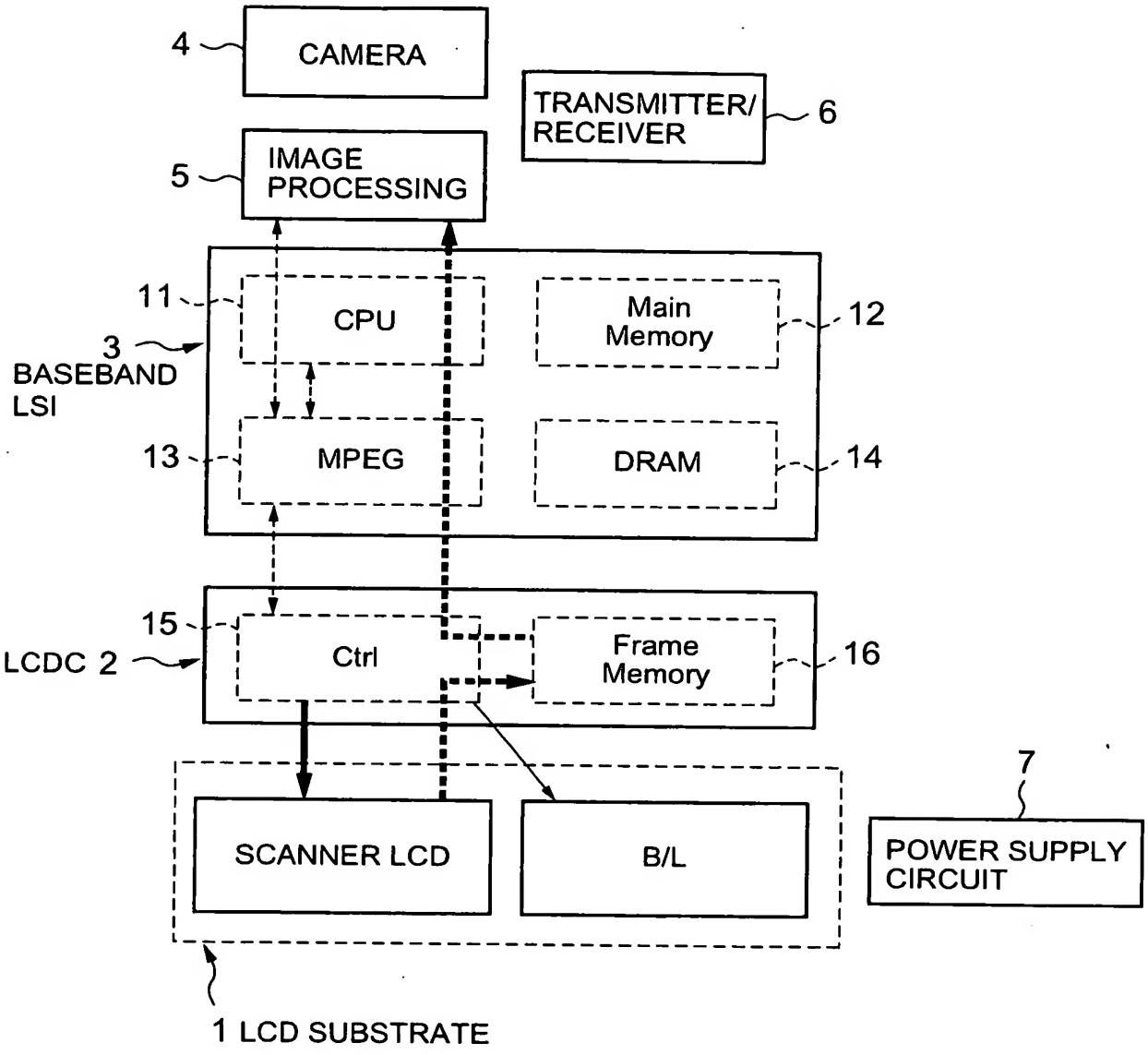

4
CAMERA
TRANSMITTER/
RECEIVER
6
5
IMAGE
PROCESSING
11
CPU
Main
Memory
12
3
BASEBAND
LSI
13
MPEG
DRAM
14
15
LCDC 2
Ctrl
Frame
Memory
16
7
SCANNER LCD
B/L
POWER SUPPLY
CIRCUIT
1 LCD SUBSTRATE

FIG.1

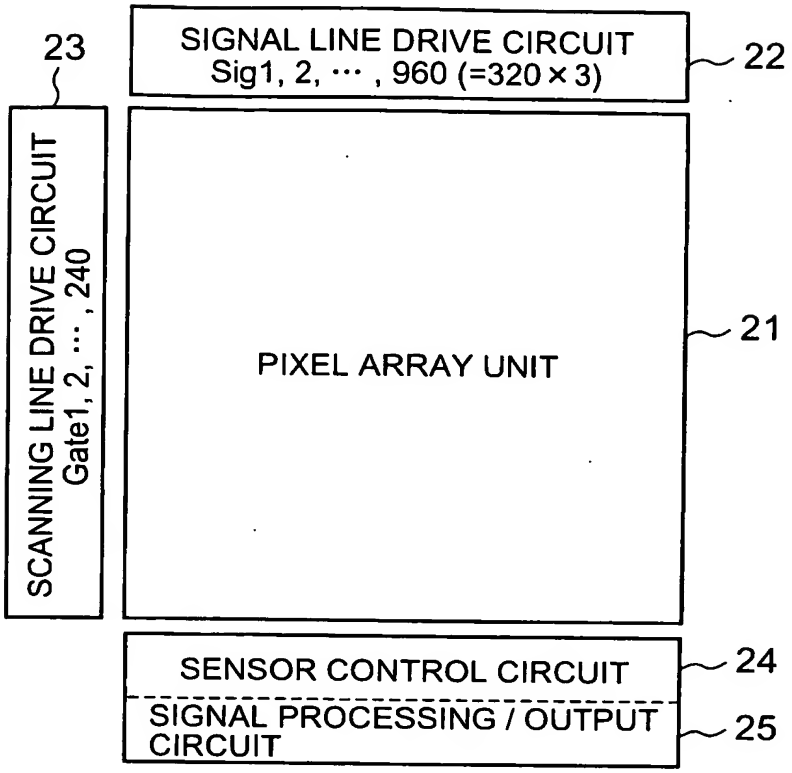

23
SIGNAL LINE DRIVE CIRCUIT
Sig1, 2, ··· , 960 (=320 × 3)
22
SCANNING LINE DRIVE CIRCUIT
Gate1, 2, ··· , 240
PIXEL ARRAY UNIT
21
SENSOR CONTROL CIRCUIT
24
SIGNAL PROCESSING / OUTPUT CIRCUIT
25

FIG.2

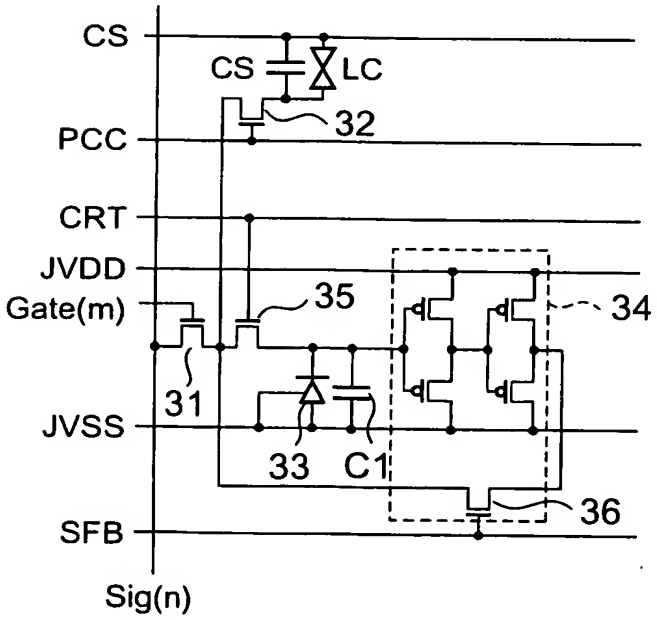

CS
CS
LC
32
PCC
CRT
JVDD
Gate(m)
35
34
31
JVSS
33
C1
36
SFB
Sig(n)

FIG.3

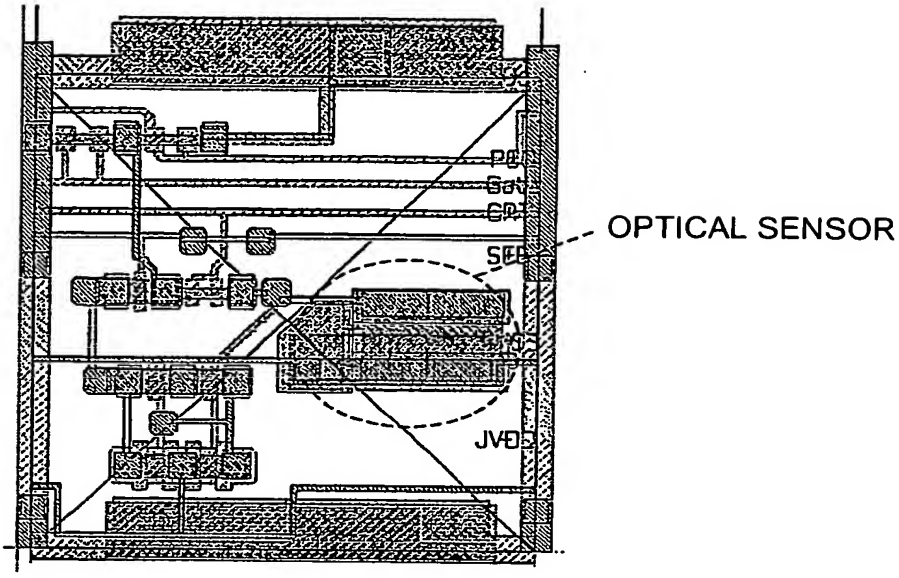

OPTICAL SENSOR

FIG.4

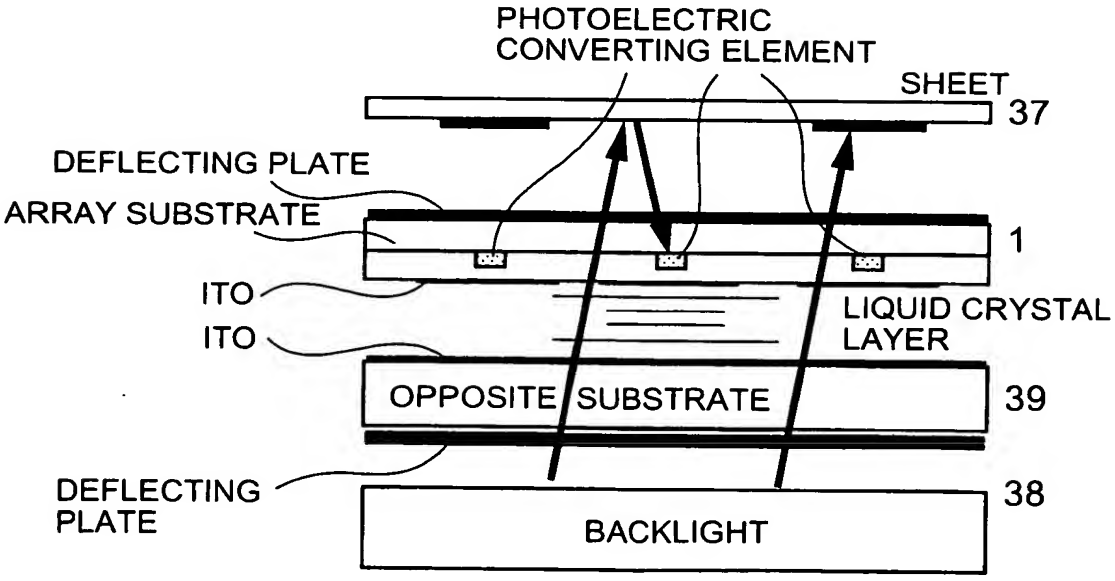

PHOTOELECTRIC
CONVERTING ELEMENT
SHEET
37
DEFLECTING PLATE
ARRAY SUBSTRATE
1
ITO
ITO
LIQUID CRYSTAL
LAYER
OPPOSITE SUBSTRATE
39
DEFLECTING
PLATE
38
BACKLIGHT

FIG.5

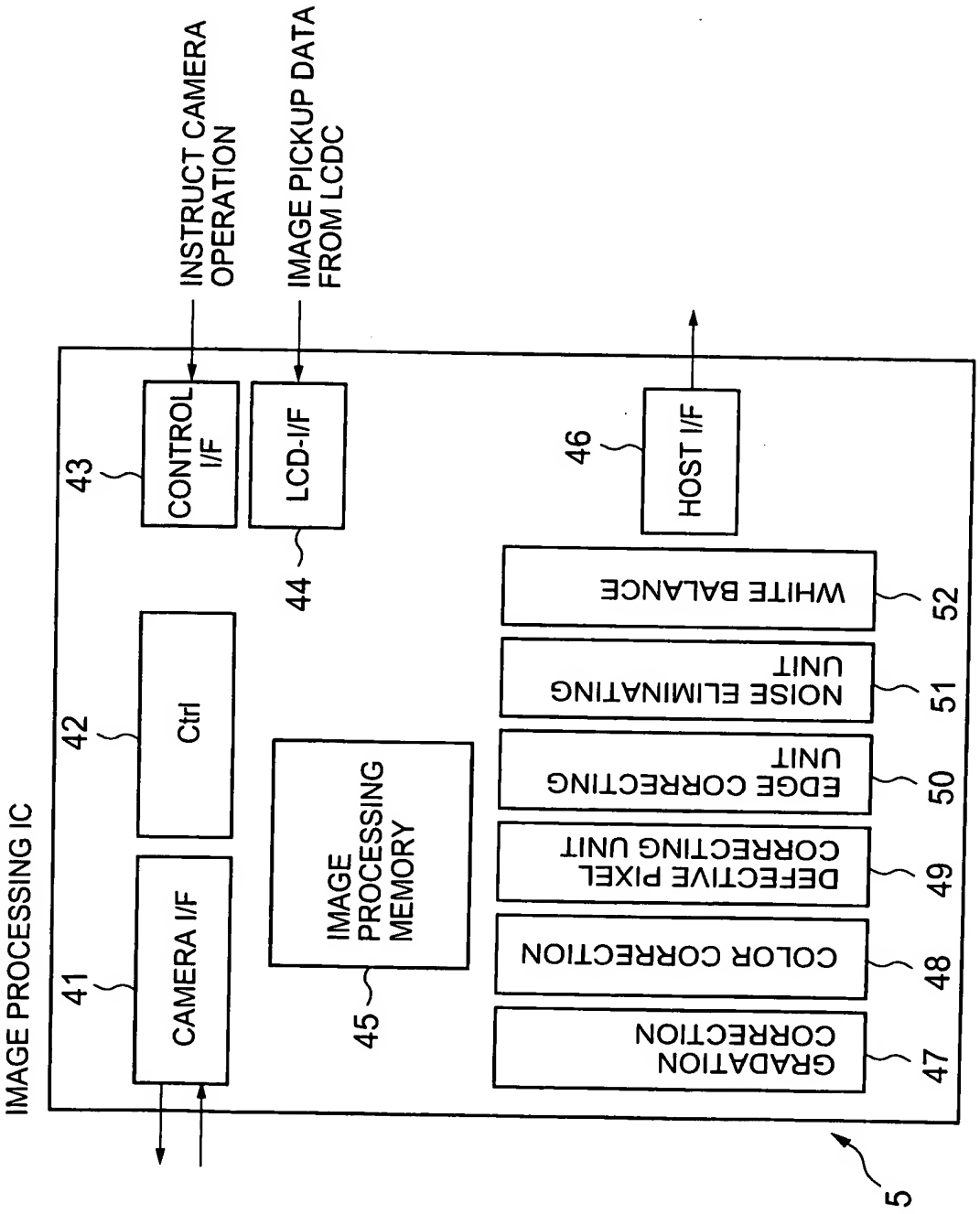

INSTRUCT CAMERA OPERATION
IMAGE PICKUP DATA FROM LCDC
IMAGE PROCESSING IC
CONTROL I/F
43
LCD-I/F
44
HOST I/F
46
Ctrl
42
IMAGE PROCESSING MEMORY
45
CAMERA I/F
41
WHITE BALANCE
52
NOISE ELIMINATING UNIT
51
EDGE CORRECTING UNIT
50
DEFECTIVE PIXEL CORRECTING UNIT
49
COLOR CORRECTION
48
GRADATION CORRECTION
47
5

FIG.6

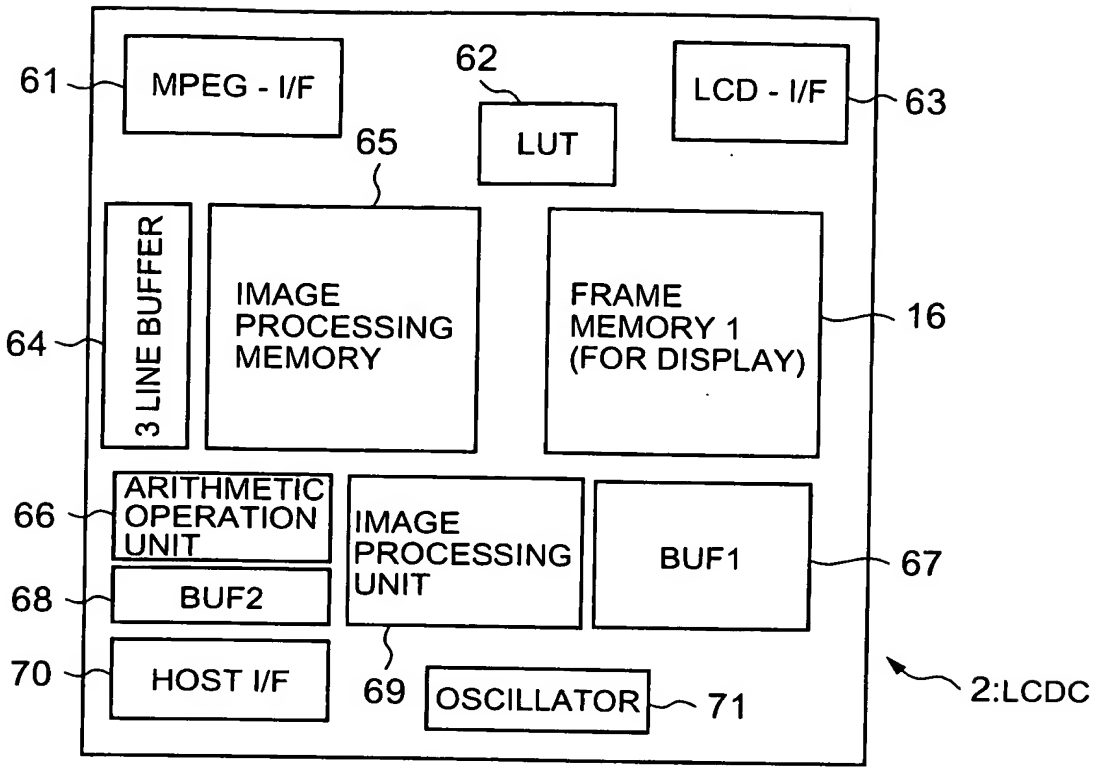

61
MPEG - I/F
62
LUT
LCD - I/F
63
65
3 LINE BUFFER
64
IMAGE PROCESSING MEMORY
FRAME MEMORY 1 (FOR DISPLAY)
16
ARITHMETIC OPERATION UNIT
66
IMAGE PROCESSING UNIT
BUF1
67
BUF2
68
HOST I/F
70
69
OSCILLATOR
71
2:LCDC

FIG.7

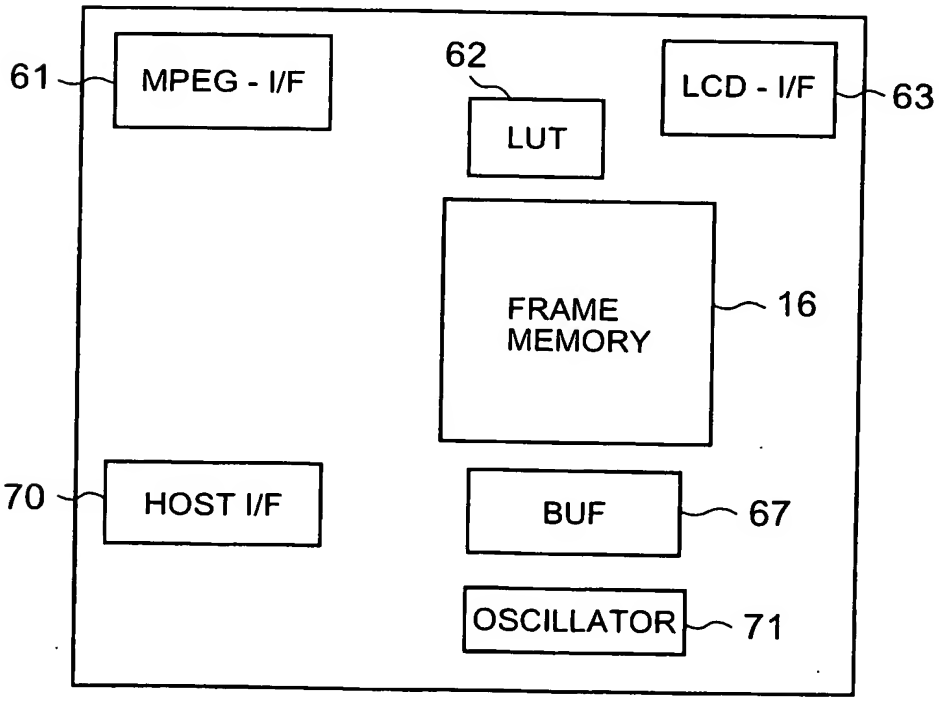

61
MPEG - I/F
62
LUT
LCD - I/F
63
FRAME MEMORY
16
70
HOST I/F
BUF
67
OSCILLATOR
71

FIG.8

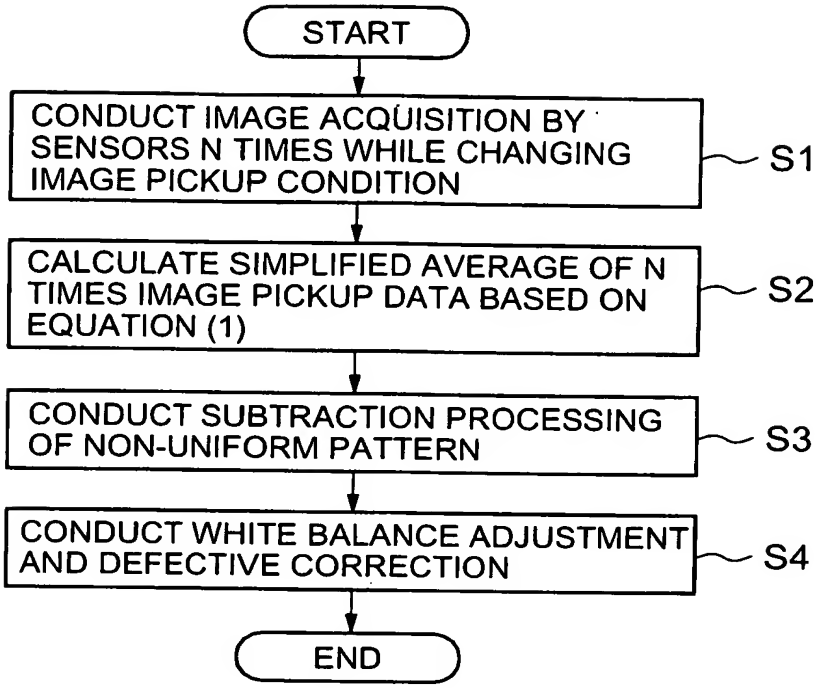

START
CONDUCT IMAGE ACQUISITION BY SENSORS N TIMES WHILE CHANGING IMAGE PICKUP CONDITION
S1
CALCULATE SIMPLIFIED AVERAGE OF N TIMES IMAGE PICKUP DATA BASED ON EQUATION (1)
S2
CONDUCT SUBTRACTION PROCESSING OF NON-UNIFORM PATTERN
S3
CONDUCT WHITE BALANCE ADJUSTMENT AND DEFECTIVE CORRECTION
S4
END

FIG.9

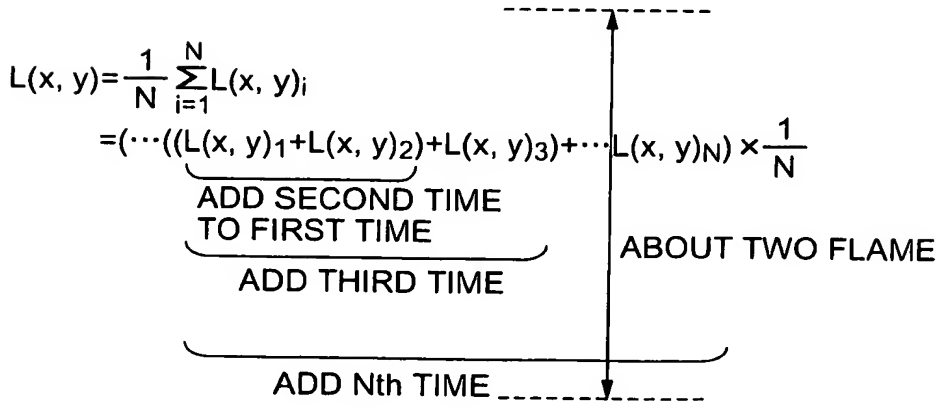

L(x, y)=1/N Σ_{i=1}^{N} L(x, y)i
=(···((L(x, y)1+L(x, y)2)+L(x, y)3)+···L(x, y)N) × 1/N
ADD SECOND TIME TO FIRST TIME
ADD THIRD TIME
ADD Nth TIME
ABOUT TWO FLAME

FIG.10

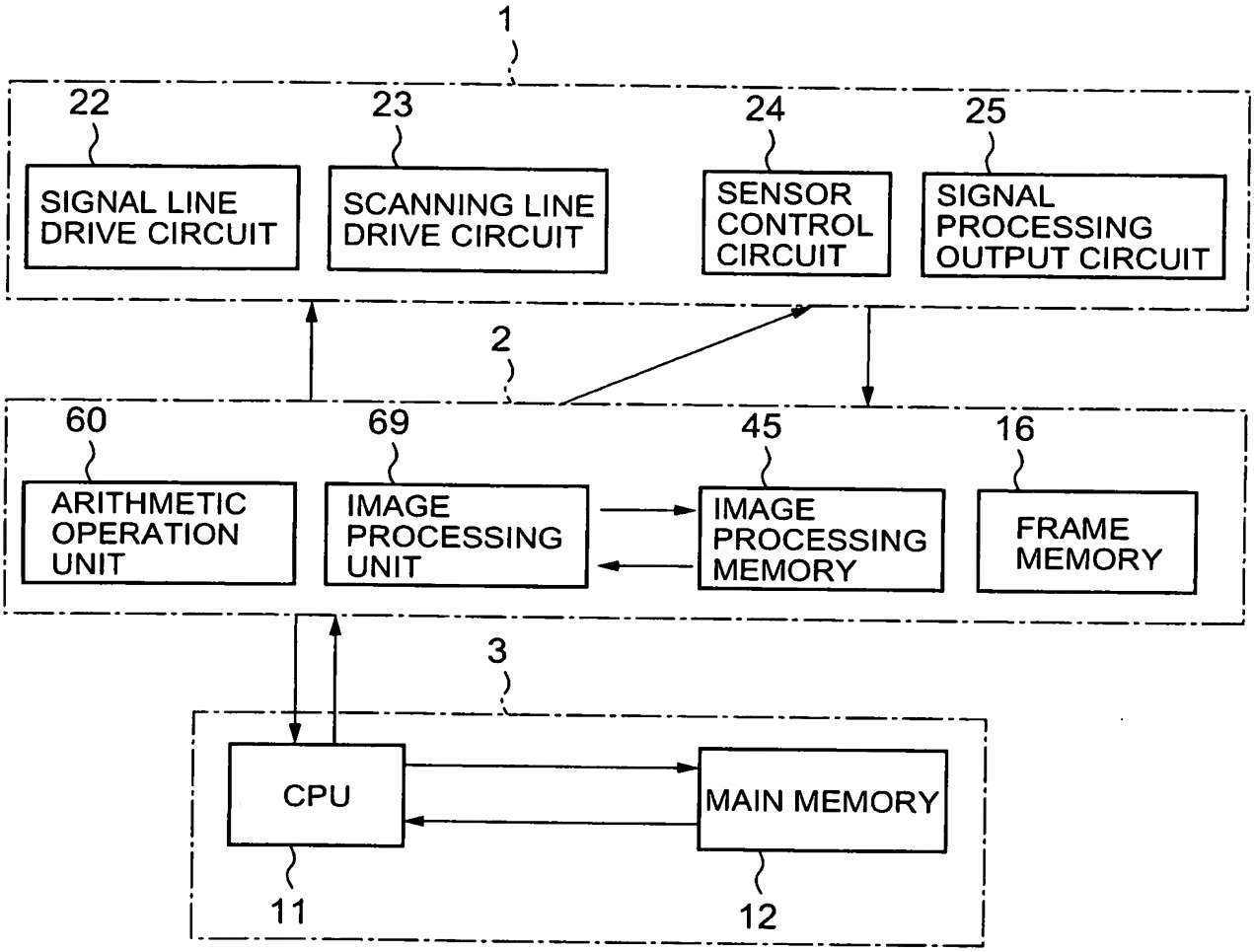

1
22
23
24
25
SIGNAL LINE DRIVE CIRCUIT
SCANNING LINE DRIVE CIRCUIT
SENSOR CONTROL CIRCUIT
SIGNAL PROCESSING OUTPUT CIRCUIT
2
60
69
45
16
ARITHMETIC OPERATION UNIT
IMAGE PROCESSING UNIT
IMAGE PROCESSING MEMORY
FRAME MEMORY
3
CPU
MAIN MEMORY
11
12

FIG.11

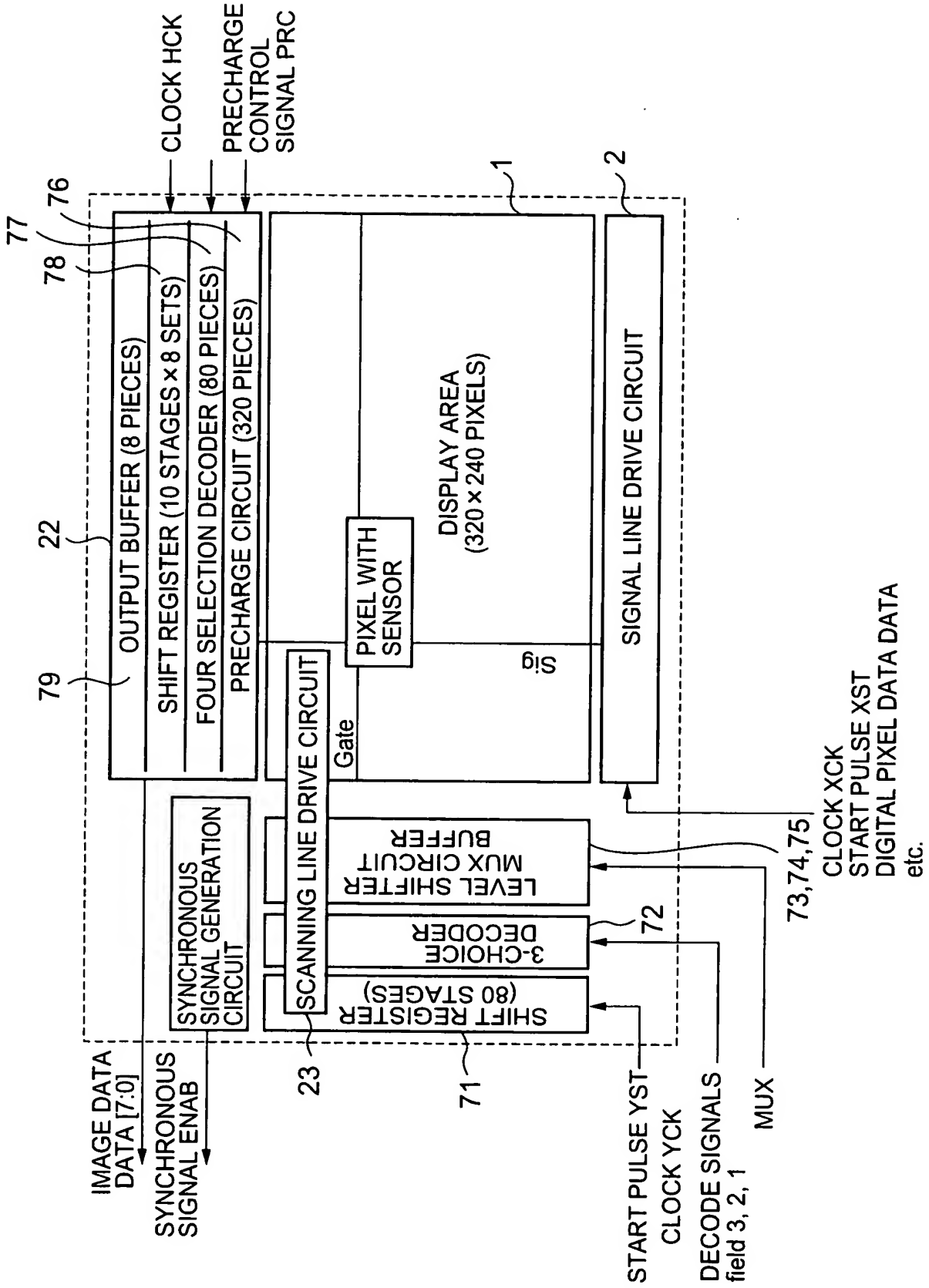

CLOCK HCK
PRECHARGE CONTROL SIGNAL PRC
77
76
78
22
79
OUTPUT BUFFER (8 PIECES)
SHIFT REGISTER (10 STAGES × 8 SETS)
FOUR SELECTION DECODER (80 PIECES)
PRECHARGE CIRCUIT (320 PIECES)
1
2
DISPLAY AREA (320 × 240 PIXELS)
PIXEL WITH SENSOR
Sig
Gate
SIGNAL LINE DRIVE CIRCUIT
SCANNING LINE DRIVE CIRCUIT
LEVEL SHIFTER MUX CIRCUIT BUFFER
3-CHOICE DECODER
72
SHIFT REGISTER (80 STAGES)
SYNCHRONOUS SIGNAL GENERATION CIRCUIT
73,74,75
CLOCK XCK
START PULSE XST
DIGITAL PIXEL DATA DATA
etc.
IMAGE DATA DATA [7:0]
SYNCHRONOUS SIGNAL ENAB
23
71
START PULSE YST
CLOCK YCK
DECODE SIGNALS field 3, 2, 1
MUX

FIG.12

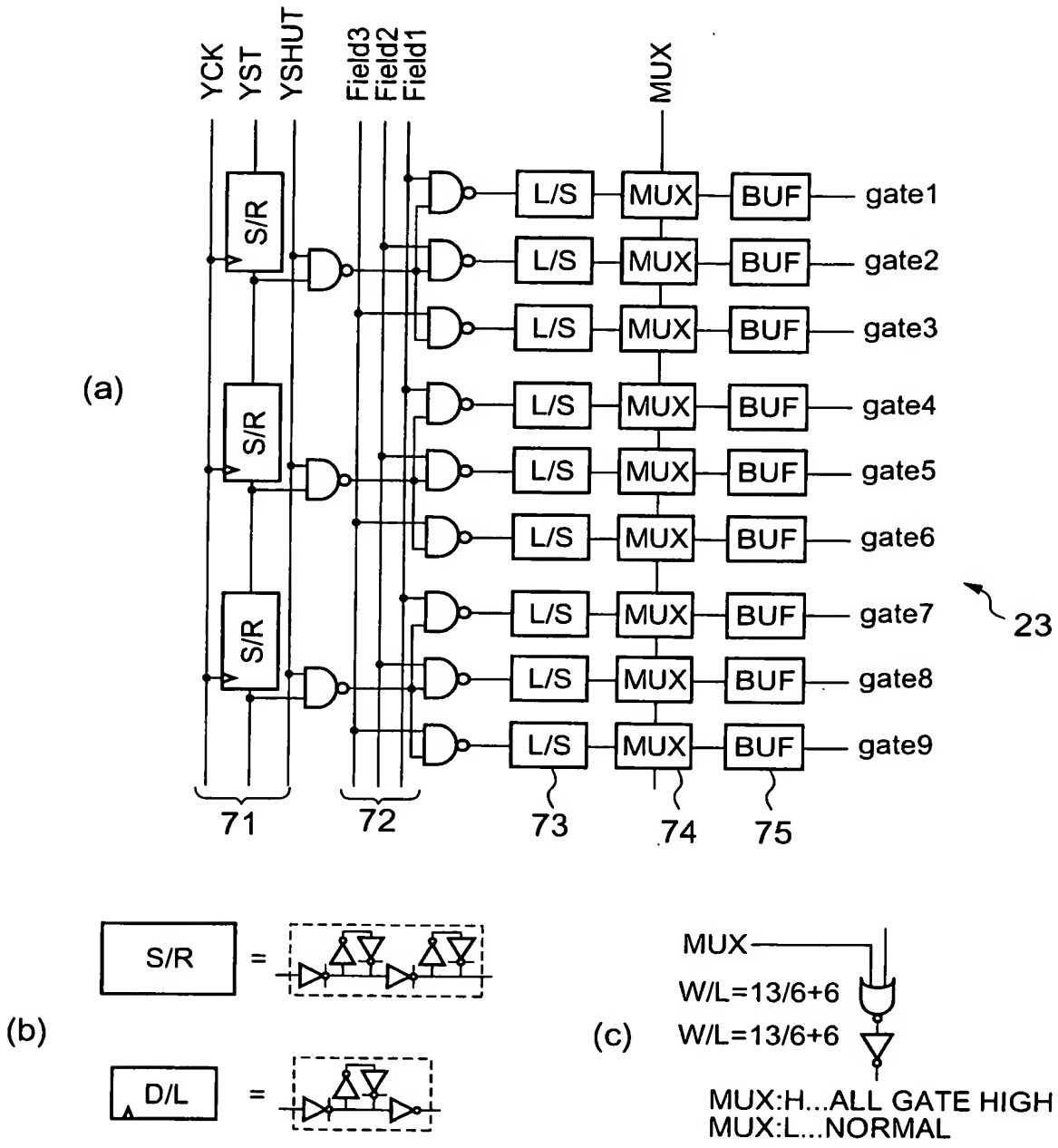

(a)
YCK
YST
YSHUT
Field3
Field2
Field1
MUX
S/R
S/R
S/R
L/S
MUX
BUF
gate1
gate2
gate3
gate4
gate5
gate6
gate7
gate8
gate9
23
71
72
73
74
75
(b)
S/R
=
D/L
=
(c)
MUX
W/L=13/6+6
W/L=13/6+6
MUX:H...ALL GATE HIGH
MUX:L...NORMAL

FIG.13

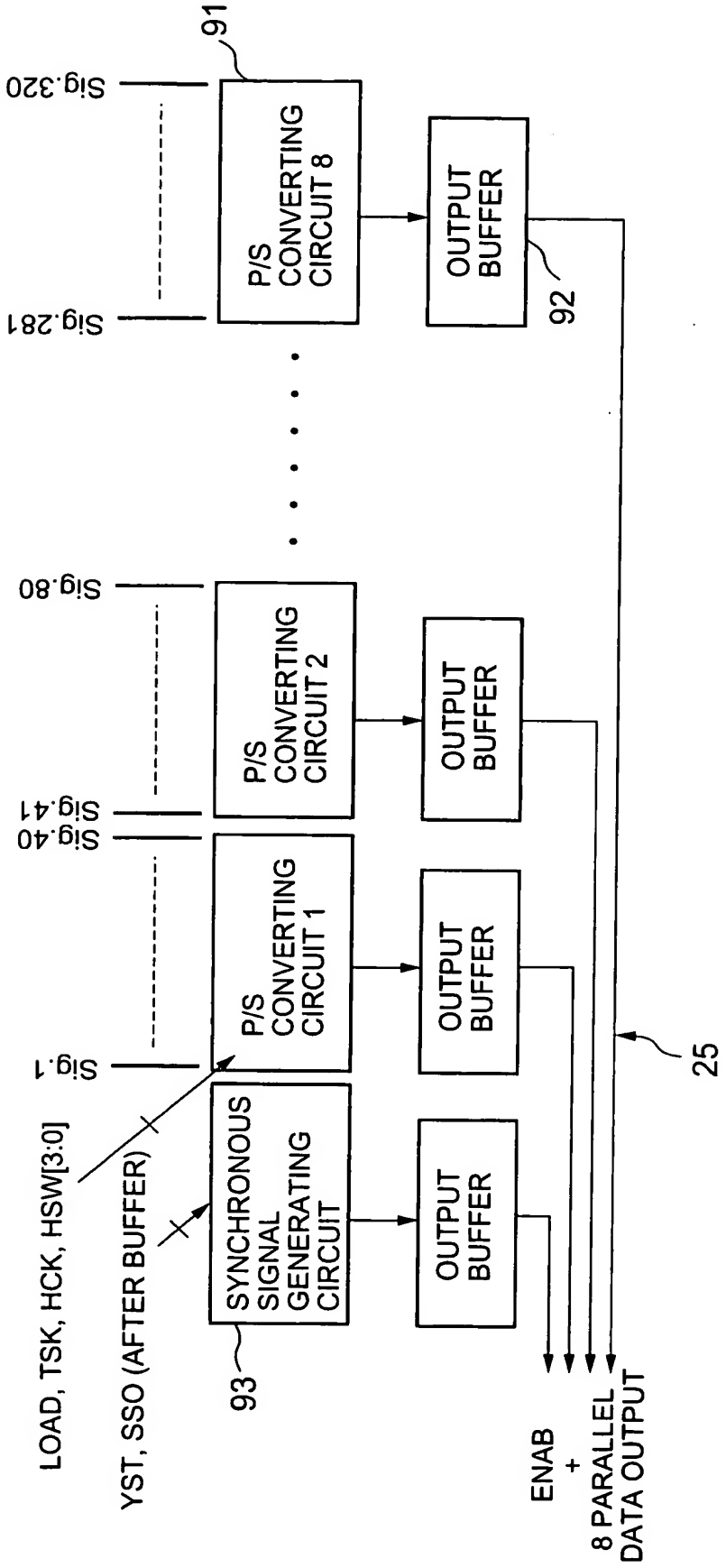

91
Sig.320
Sig.281
P/S CONVERTING CIRCUIT 8
OUTPUT BUFFER
92
Sig.80
Sig.41
Sig.40
Sig.1
P/S CONVERTING CIRCUIT 2
P/S CONVERTING CIRCUIT 1
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
25
LOAD, TSK, HCK, HSW[3:0]
YST, SSO (AFTER BUFFER)
SYNCHRONOUS SIGNAL GENERATING CIRCUIT
93
ENAB
+
8 PARALLEL DATA OUTPUT

FIG.14

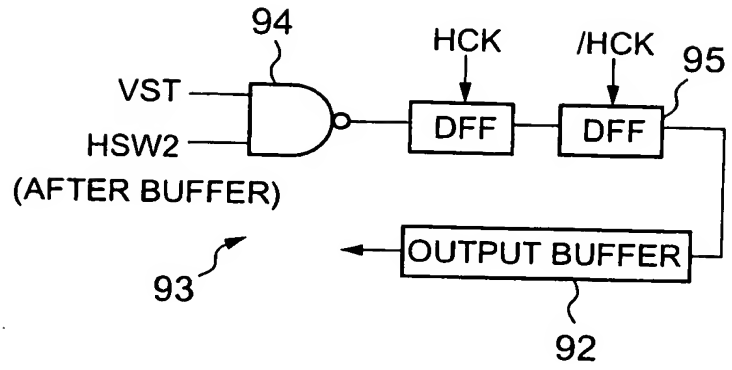

94
HCK
/HCK
95
VST
HSW2
(AFTER BUFFER)
DFF
DFF
OUTPUT BUFFER
93
92

FIG.15

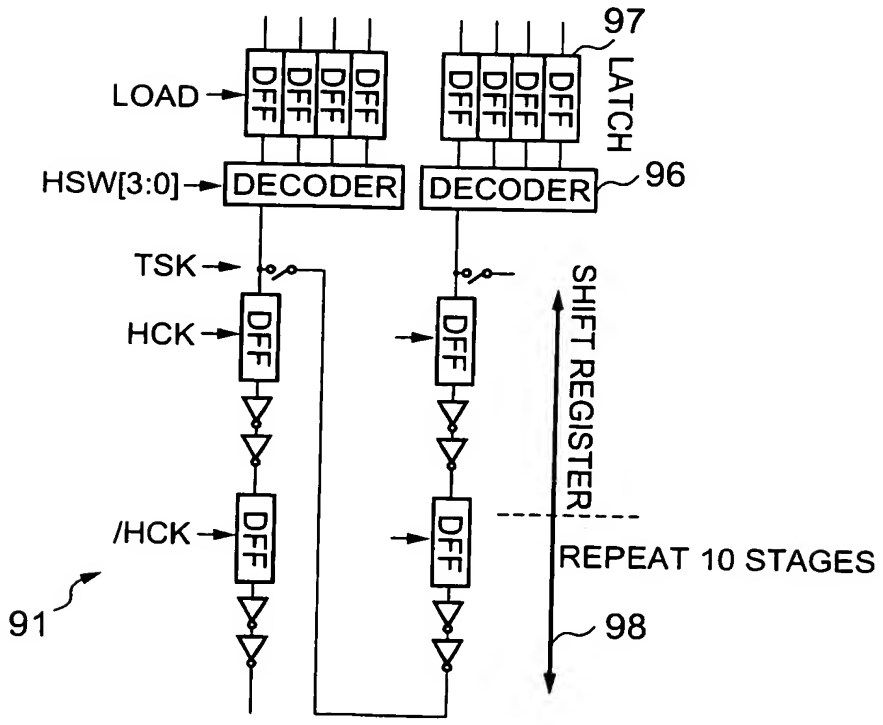

97
LATCH
LOAD
HSW[3:0]
DECODER
DECODER
96
TSK
HCK
/HCK
DFF
SHIFT REGISTER
REPEAT 10 STAGES
91
98

FIG.16

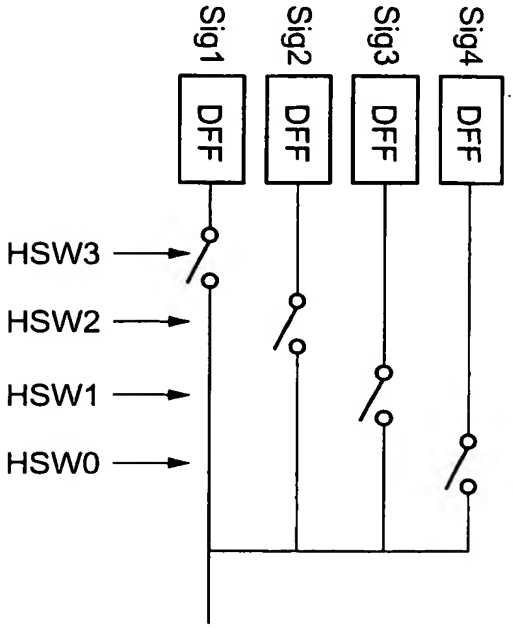


FIG.17

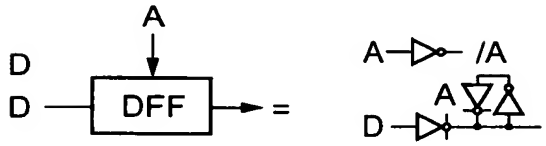


FIG.18

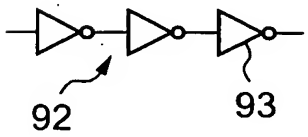


FIG.19

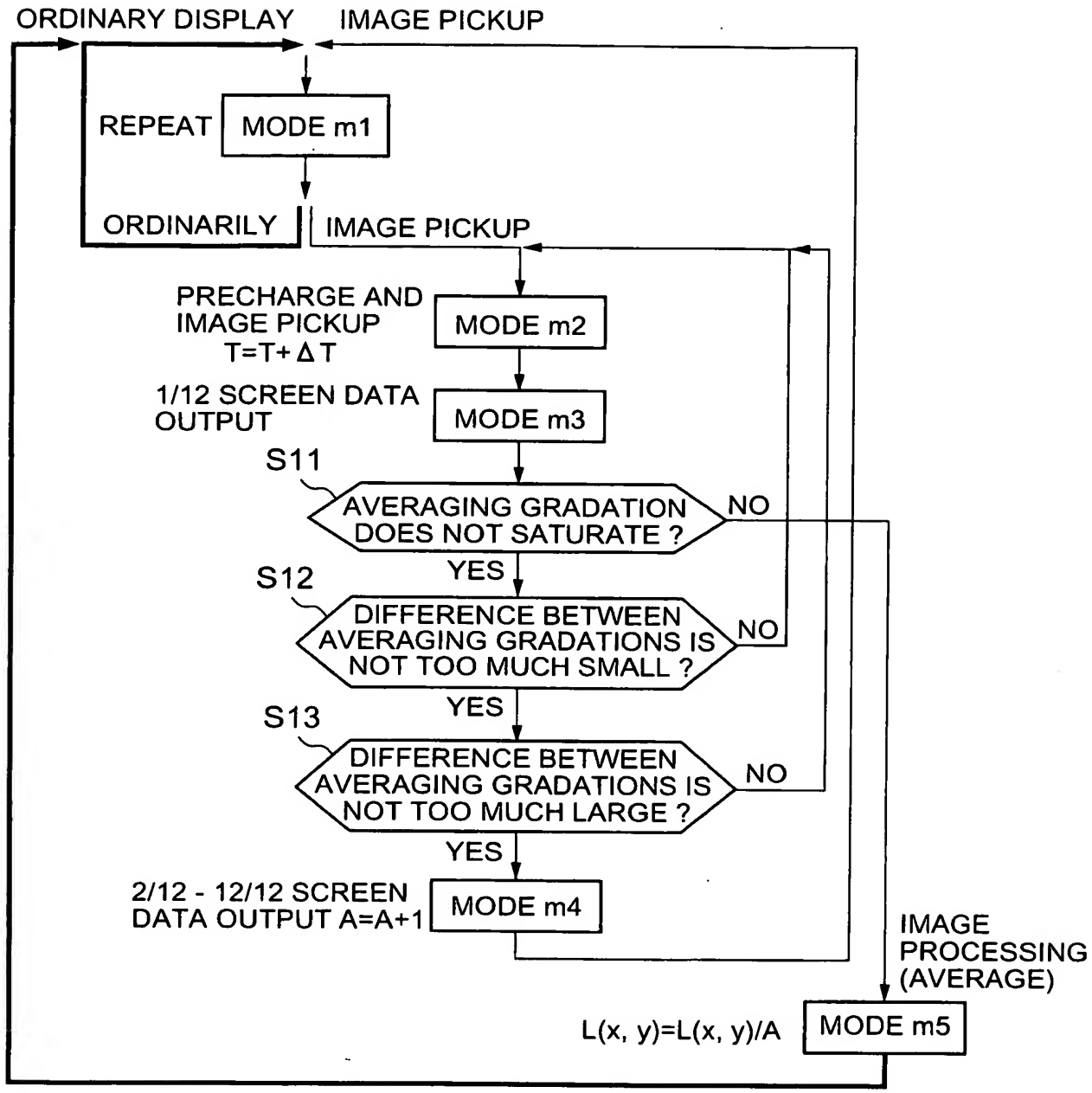

ORDINARY DISPLAY
IMAGE PICKUP
REPEAT
MODE m1
ORDINARILY
IMAGE PICKUP
PRECHARGE AND IMAGE PICKUP T=T+ΔT
MODE m2
1/12 SCREEN DATA OUTPUT
MODE m3
S11
AVERAGING GRADATION DOES NOT SATURATE ?
NO
YES
S12
DIFFERENCE BETWEEN AVERAGING GRADATIONS IS NOT TOO MUCH SMALL ?
NO
YES
S13
DIFFERENCE BETWEEN AVERAGING GRADATIONS IS NOT TOO MUCH LARGE ?
NO
YES
2/12 - 12/12 SCREEN DATA OUTPUT A=A+1
MODE m4
IMAGE PROCESSING (AVERAGE)
L(x, y)=L(x, y)/A
MODE m5

FIG.20

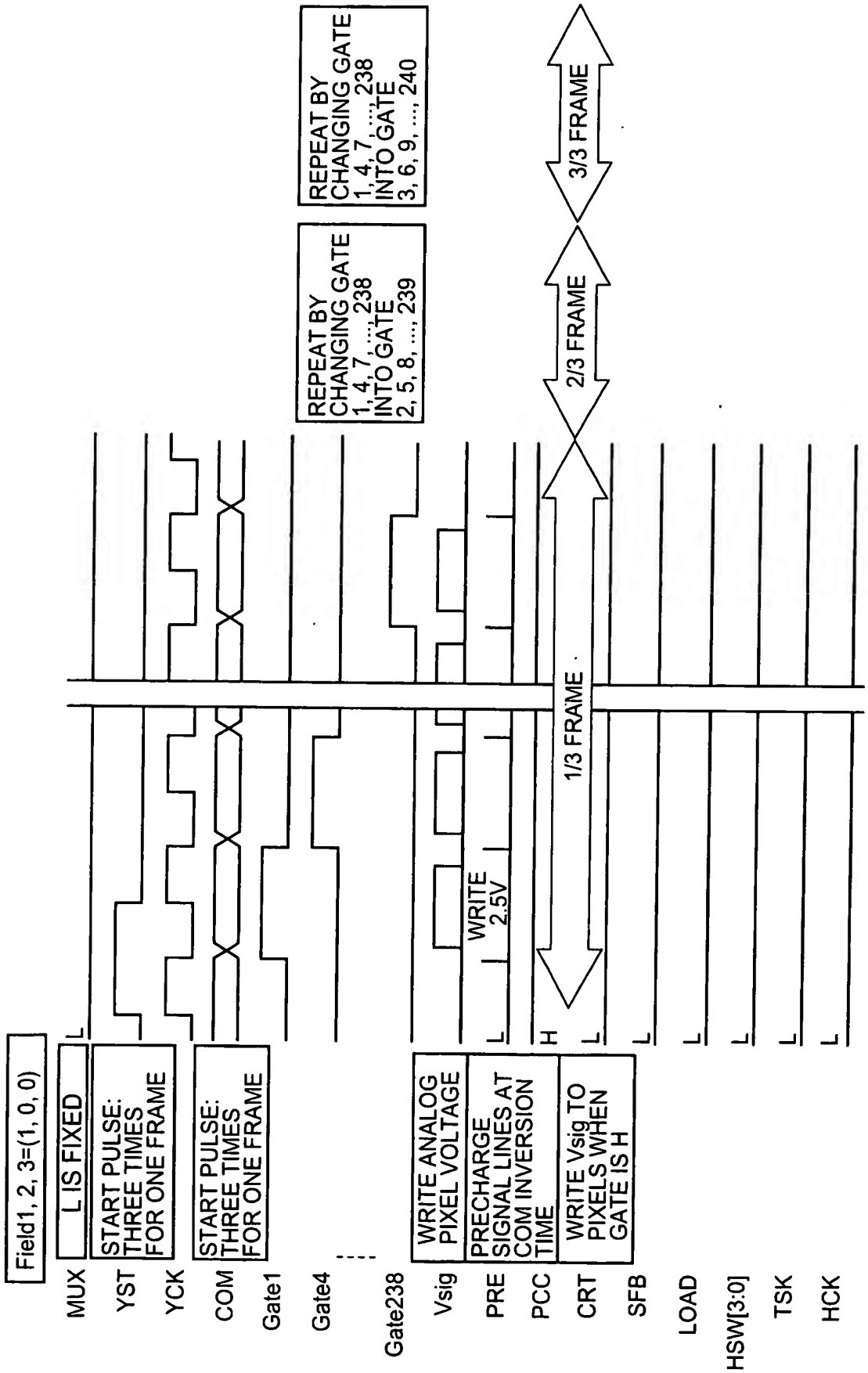

Field1, 2, 3=(1, 0, 0)
MUX
YST
YCK
COM
Gate1
Gate4
Gate238
Vsig
PRE
PCC
CRT
SFB
LOAD
HSW[3:0]
TSK
HCK
L IS FIXED
START PULSE: THREE TIMES FOR ONE FRAME
START PULSE: THREE TIMES FOR ONE FRAME
WRITE ANALOG PIXEL VOLTAGE
PRECHARGE SIGNAL LINES AT COM INVERSION TIME
WRITE Vsig TO PIXELS WHEN GATE IS H
WRITE 2.5V
1/3 FRAME
2/3 FRAME
3/3 FRAME
REPEAT BY CHANGING GATE 1, 4, 7, ..., 238 INTO GATE 2, 5, 8, ..., 239
REPEAT BY CHANGING GATE 1, 4, 7, ..., 238 INTO GATE 3, 6, 9, ..., 240
L
H

FIG.21

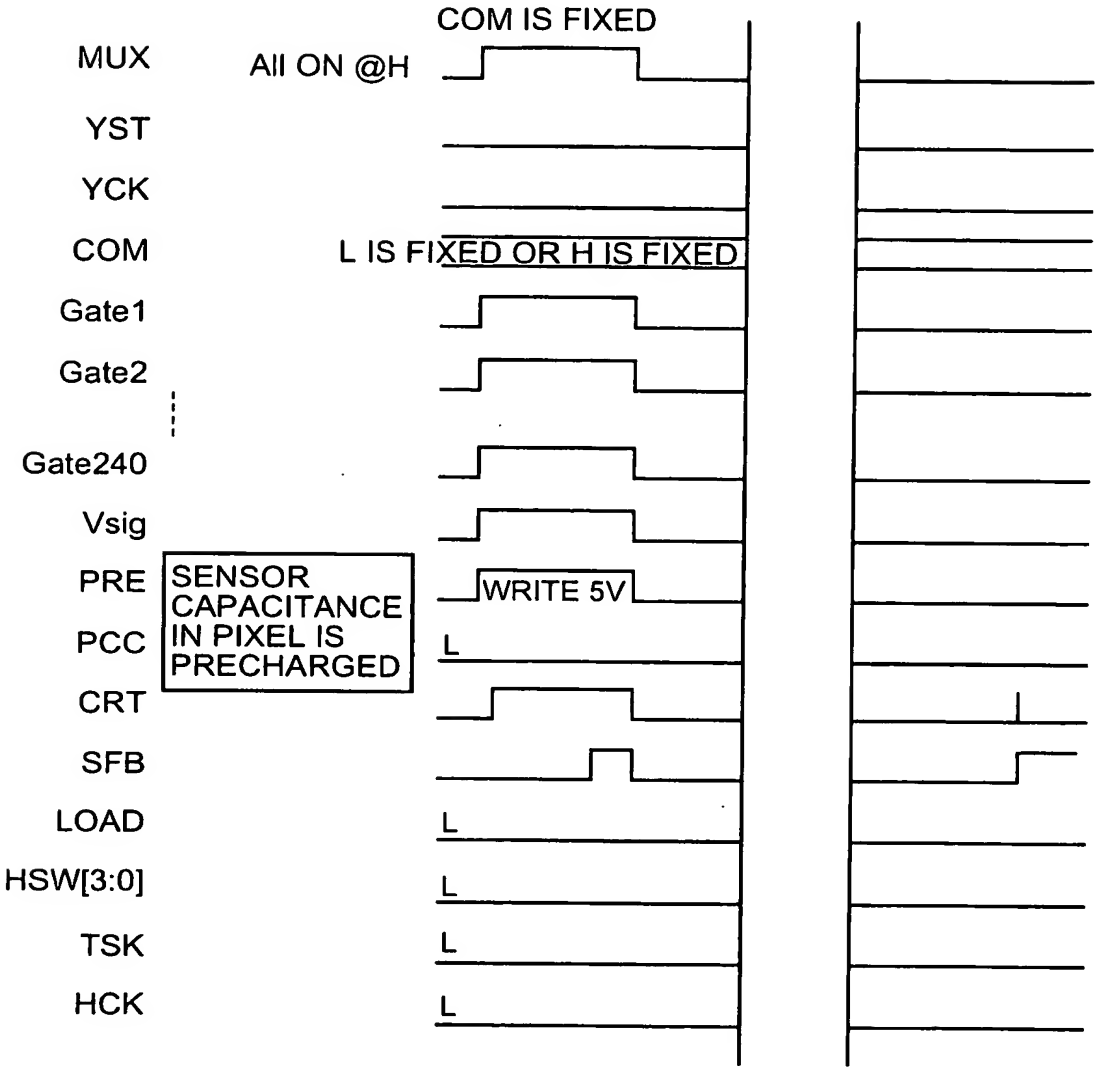
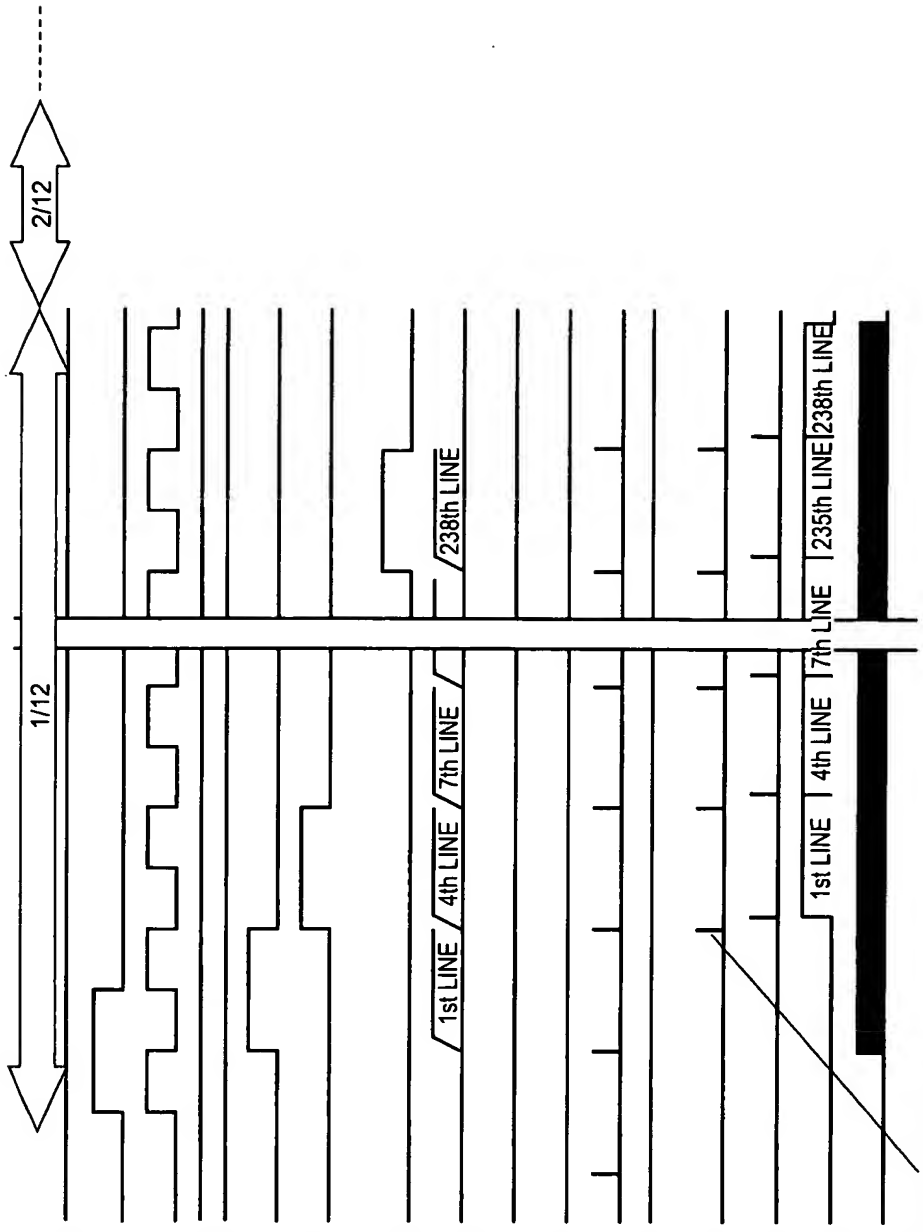

COM IS FIXED
MUX
All ON @H
YST
YCK
COM
L IS FIXED OR H IS FIXED
Gate1
Gate2
Gate240
Vsig
PRE
SENSOR CAPACITANCE IN PIXEL IS PRECHARGED
WRITE 5V
PCC
L
CRT
SFB
LOAD
L
HSW[3:0]
L
TSK
L
HCK
L

FIG.22

16/22



LATCH DATA OF FIRST LINE

REPEAT 12 TIMES (LIST OF PARAMETERS)

	1/12	2/12	3/12	4/12	5/12	6/12	7/12	8/12	9/12	10/12	11/12	12/12
gate1	1					2			3			
gate4	4					5			6			
gate238	238					239			240			
HSW[3:0]	1,0,0,0	0,1,0,0	0,0,1,0	0,0,0,1	1,0,0,0	0,1,0,0	0,0,1,0	0,0,0,1	1,0,0,0	0,1,0,0	0,0,1,0	0,0,0,1

FIG.23

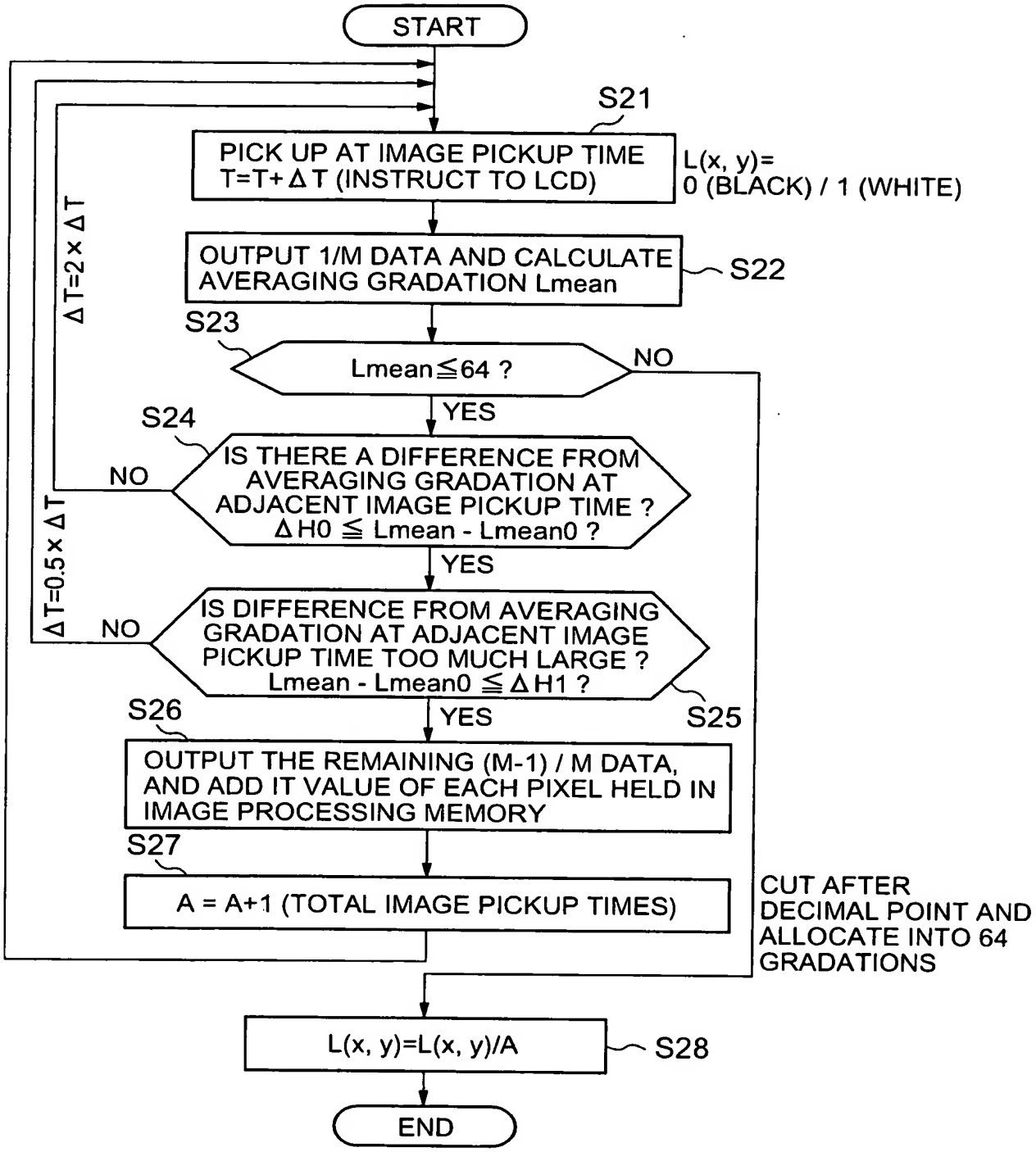

START
S21
PICK UP AT IMAGE PICKUP TIME
T=T+ΔT (INSTRUCT TO LCD)
L(x, y)=
0 (BLACK) / 1 (WHITE)
OUTPUT 1/M DATA AND CALCULATE
AVERAGING GRADATION Lmean
S22
S23
Lmean≦64 ?
NO
YES
S24
IS THERE A DIFFERENCE FROM
AVERAGING GRADATION AT
ADJACENT IMAGE PICKUP TIME ?
ΔH0 ≦ Lmean - Lmean0 ?
NO
YES
IS DIFFERENCE FROM AVERAGING
GRADATION AT ADJACENT IMAGE
PICKUP TIME TOO MUCH LARGE ?
Lmean - Lmean0 ≦ ΔH1 ?
NO
YES
S25
S26
OUTPUT THE REMAINING (M-1) / M DATA,
AND ADD IT VALUE OF EACH PIXEL HELD IN
IMAGE PROCESSING MEMORY
S27
A = A+1 (TOTAL IMAGE PICKUP TIMES)
ΔT=2×ΔT
ΔT=0.5×ΔT
CUT AFTER
DECIMAL POINT AND
ALLOCATE INTO 64
GRADATIONS
L(x, y)=L(x, y)/A
S28
END

FIG.24

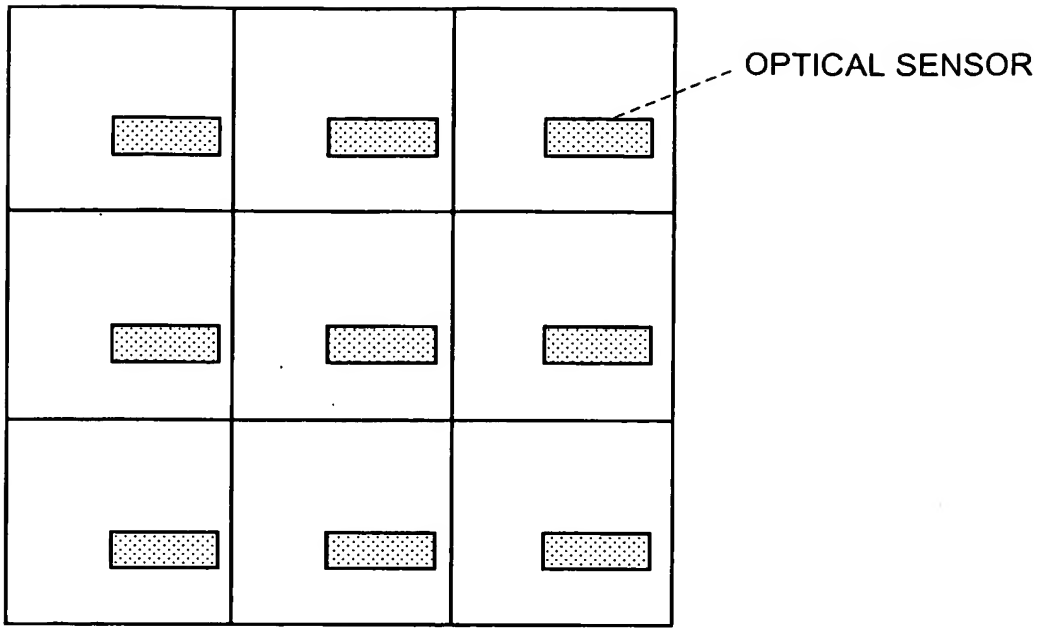

OPTICAL SENSOR

FIG.25

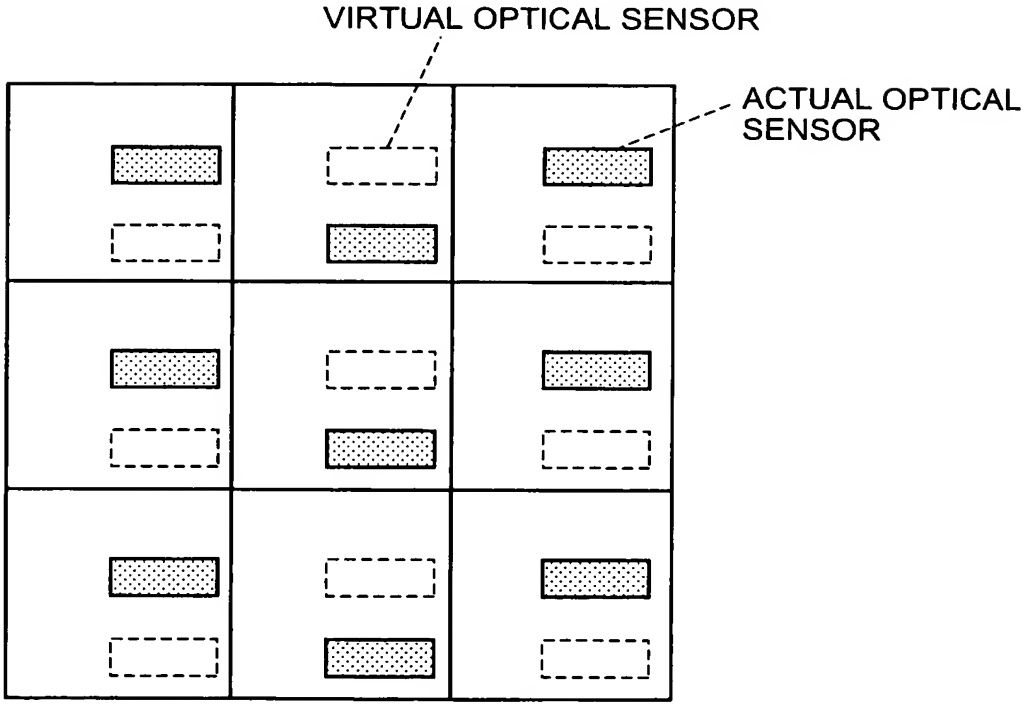

VIRTUAL OPTICAL SENSOR
ACTUAL OPTICAL SENSOR

FIG.26

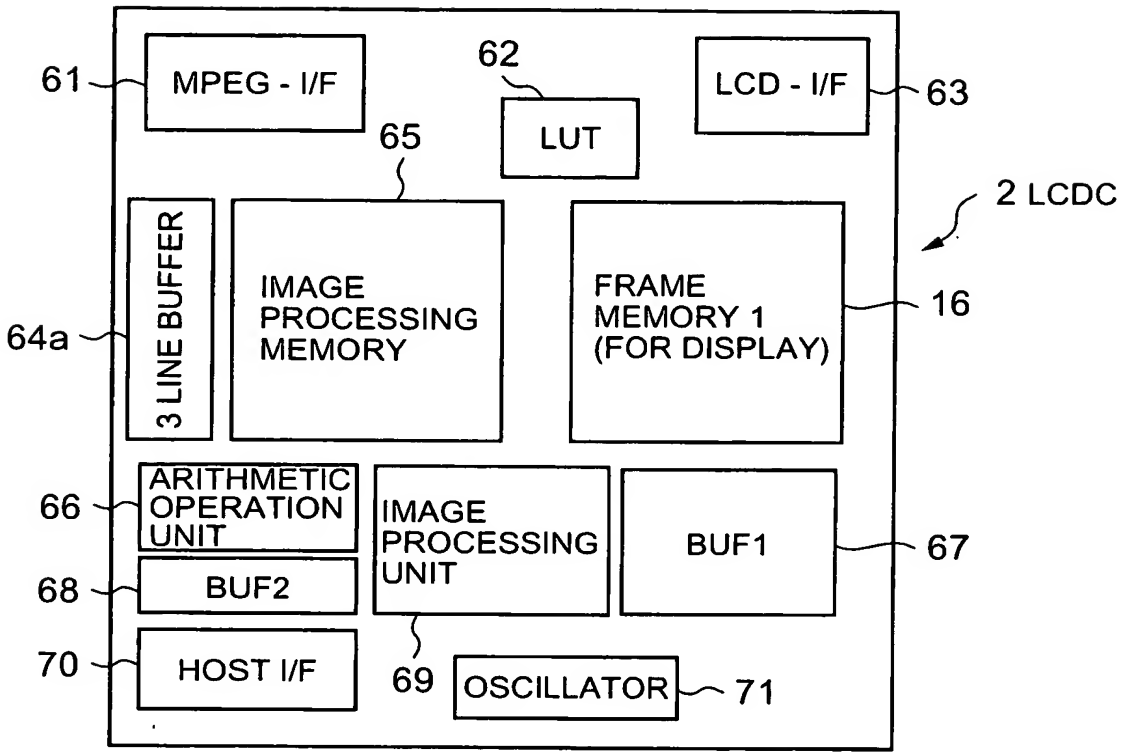

61
MPEG - I/F
62
LUT
LCD - I/F
63
65
2 LCDC
64a
3 LINE BUFFER
IMAGE PROCESSING MEMORY
FRAME MEMORY 1 (FOR DISPLAY)
16
66
ARITHMETIC OPERATION UNIT
IMAGE PROCESSING UNIT
BUF1
67
68
BUF2
70
HOST I/F
69
OSCILLATOR
71

FIG.27

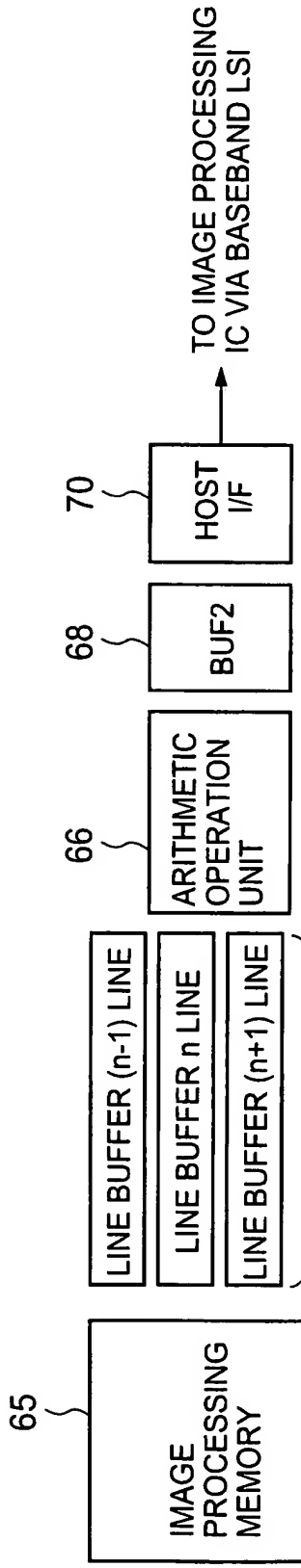

65
IMAGE PROCESSING MEMORY
LINE BUFFER (n-1) LINE
LINE BUFFER n LINE
LINE BUFFER (n+1) LINE
64a
66
ARITHMETIC OPERATION UNIT
68
BUF2
70
HOST I/F
TO IMAGE PROCESSING IC VIA BASEBAND LSI

FIG.28

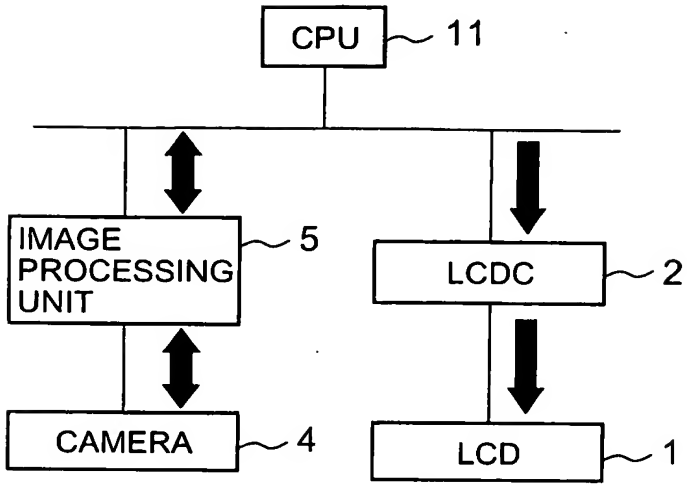

CPU
11
IMAGE PROCESSING UNIT
5
LCDC
2
CAMERA
4
LCD
1

FIG.29

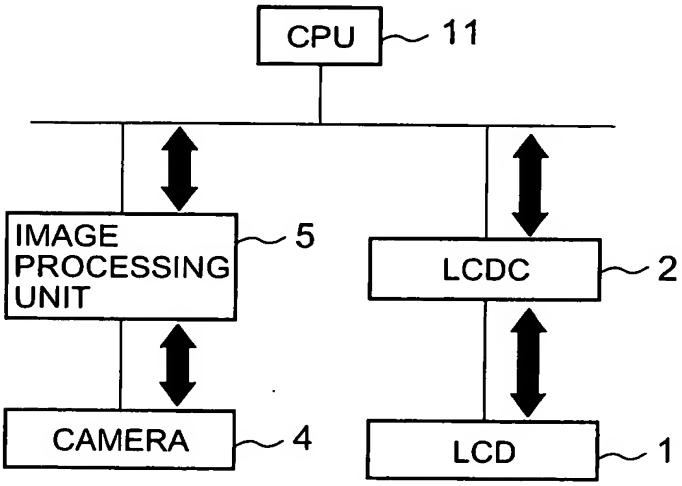

CPU
11
IMAGE PROCESSING UNIT
5
LCDC
2
CAMERA
4
LCD
1

FIG.30

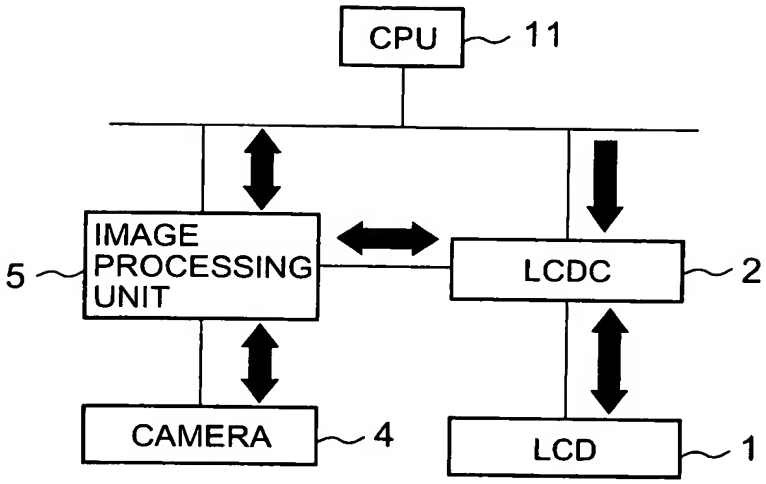


FIG.31